

COMPARISON OF DESIGNING BUTTERFLY TYPED FFT BLOCK IN MIMO - OFDM SYSTEM USING PIPELINE ARCHITECTURE

SO SÁNH THIẾT KẾ KHỐI FFT KIỂU BUTTERFLY TRONG HỆ THỐNG MIMO - OFDM SỬ DỤNG KIẾN TRÚC ĐƯỜNG DẪN PIPELINE

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Tóm tắt:

MIMO (Multiple Input - Multiple Output) - OFDM (Orthogonal Frequency Devision Multiplex) system using FPGA (Field-Programmable Gate Array) is researched extensively at the moment. The architecture of this system is mainly based on the base, which uses two IFFT (Inverse Fast Fourier Transform) blocks connected to two antennas. However, this architecture wil waste the resources. The paper concentrates on researching the pipeline architecture that utilize only one IFFT block for two antennas, especially butterfly type. Two design schematics are used, including Sysgen and direct Vivado. The first architecture guarantees the function of the signal processing like the latter while using less the resource.

Từ khóa:

Butterfly type FFT block, MIMO - OFDM, FPGA.

Abstract:

Hệ thống đa đầu vào - đa đầu ra MIMO - ghép kênh theo tần số trực giao OFDM sử dụng ma trận cổng có khả năng lập trình trên chip (FPGA) được nghiên cứu nhiều trong thời gian hiện nay. Kiến trúc của hệ thống này chủ yếu dựa trên cơ sở, sử dụng hai khối biến đổi biến đổi Fourier nhanh ngược (IFFT) cho 2 anten. Tuy nhiên, kiến trúc này sẽ lãng phí nguồn tài nguyên sử dụng. Bài báo tập trung nghiên cứu sử dụng kiến trúc đường dẫn (pipeline), trong đó chỉ sử dụng một khối IFFT cho hai anten (kiểu butterfly đặc biệt). Hai sơ đồ thiết kế được đưa ra cho khối IFFT này, sử dụng Sysgen và Vivado trực tiếp. Kiến trúc trước vẫn đảm bảo chức năng xử lý tín hiệu như kiến trúc trước nhưng nguồn tài nguyên sử dụng sẽ ít đi.

Keywords:

Khối FFT kiểu Buterfly, MIMO - OFDM, FPGA.

1. GIỚI THIỆU CHUNG

SDM (Spatial Multiplexing Technology) is being paid much attention to improving the use of spectrum resources and transmission speed for modern radio

networks. The basis of SDM technology is the use of MIMO technology that uses multiple transmitting and receiving antennas to divide the space into independent transmission subspaces. A

combination of MIMO technology and OFDM orthogonal frequency division multiple access technology will further improve the transmission speed. However, the research focuses on analyzing and evaluating system quality based on theory and simulation. Very little research on the design and implementation of the MIMO - OFDM system based on FPGA, is an important basis for manufacturing practical IC circuits [1]. The design schematics in this paper still focus on basic FFT (Fast Fourier Transform)/ IFFT (Invert Fast Fourier Transform) signal processing.

Currently, FPGA technology in the world is being used to manufacture high-tech signal processing equipment, including FFT/IFFT transform using pipeline [2], [3]. This is a good approach in the MIMO - OFDM transmission system. The authors also base on this design applied to MIMO - OFDM transmission system using pipelined FFT/IFFT, combined with Verilog language in [5].

2. FUNCTIONAL BLOCKS IN BASELINE FPGA SYSTEM

We describe the functional block schematic of the MIMO - OFDM system used in the paper and their functions.

The first data block of interest is the $N \times M$ MIMO - OFDM block: N is the number of transmitting antennas and M is the number of receiving antennas, respectively. For example, in Figure 1, MIMO - OFDM 2×2 has two transmitting and two receiving antennas. For MIMO - OFDM systems, the baseline uses multiple IFFT (or FFT) depending on the

number of antennas at the transmitter (or receiver). This simple idea is consistent with the basic theory of MIMO - OFDM recommends that many data streams are modulated by their own IFFT blocks.

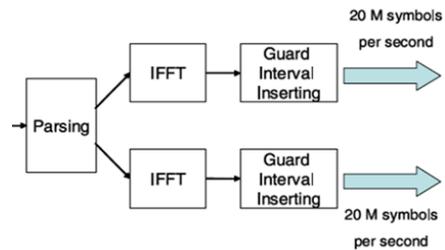


Figure 1. Transmit and receive data flows (complex symbol 32 bit)

3. DESIGN OF IMPROVED MIMO - OFDM SYSTEM USING PIPELINE TECHNIQUE ON FPGA

The detailed block schematic shows the blocks, pipeline phase and data flows given by Figure 2. The pipeline phase has a time of $4 \mu\text{s}$. In addition, $4 \mu\text{s}$ is suitable for the pipeline stage because the transmission time for a group of modulated data is $4 \mu\text{s}$. Therefore, 4-stage pipeline architecture for each stage is a good design solution for MIMO - OFDM transceiver.

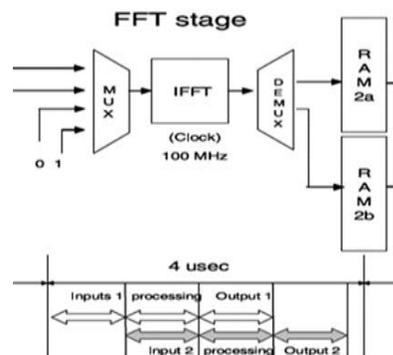


Figure 2. Improved pipeline technique

Example of IFFT processing schematic using pipeline based on the above idea:

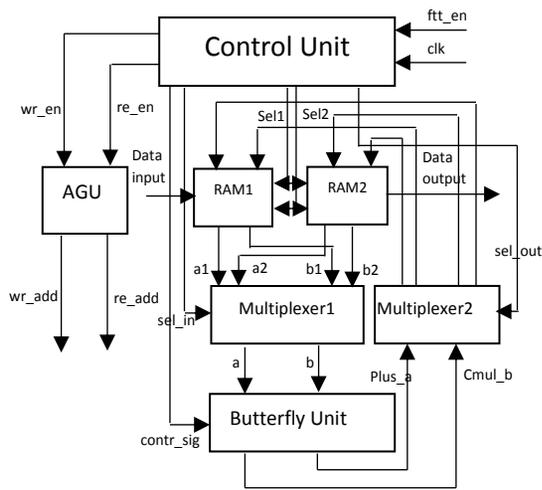


Figure 3. IFFT schematic using FPGA

4. SCHEMATIC IMPLEMENTING IFFT BUTTERFLY BLOCKS

Schematic 1:

We can create Butterfly (BU) blocks

based on the Sysgen (System Generation) schematic in Matlab, then convert to the Xilinx Vivado system. We have the implementation schematic for the Radix - 2 butterfly block and the resources used as shown in Figure 5.

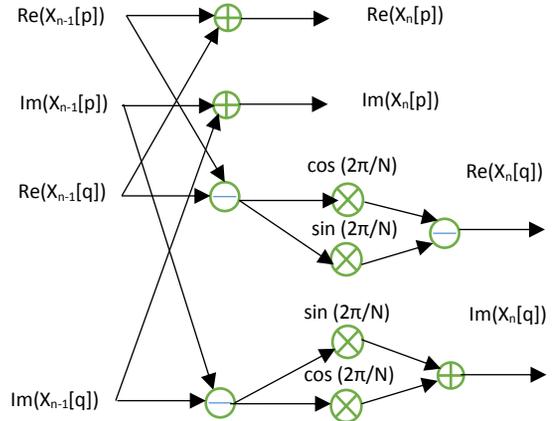


Figure 4. The first functional diagram for Butterfly Radix - 2 block

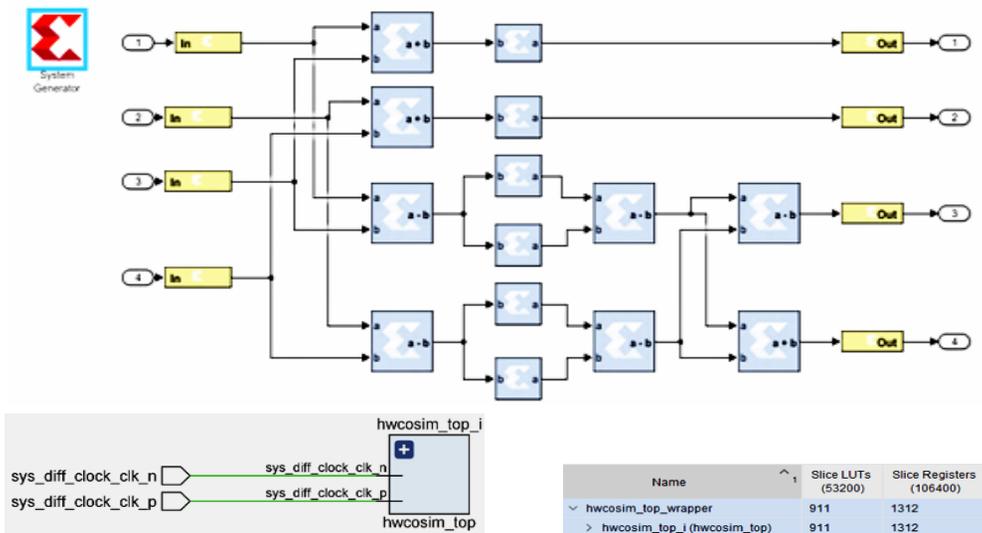


Figure 5. Butterfly Radix-2 implementing schematic using Sysgen (schematic 1)

Schematic 2:

Through the use of Xilinx Vivado software, we obtain the principle schematic as shown in Figure 7. The resource usage table for the principle schematic of Figure 7 is depicted by Figure 8.

The schematics are simulated by the author based on functional diagrams in Figures 4 and 6. These two functional diagrams are for two-input, two-output IFFT transforms. It can be seen from Figures 4 and 6 that they all have the same function of performing the Butterfly

diagram in the IFFT transform. However, we use the advantage of the Sysgen system in Matlab when Xilinx System Generator (XSG or Sysgen) is a tool which offers block libraries that plugs into simulink tool to create HDL (Hardware Description Language) designs from MATLAB. It provides many features such as system resource estimation to take full advantage of FPGA resources, hardware co-simulation and accelerated simulation through hardware in the loop co-simulation which give many orders of simulation performance increase. The Sysgen diagram only uses the basic

blocks AddSub (8 blocks - 4 blocks in, 4 out) and BitBasher (4 blocks in the middle) as shown in Figure 5. These are the blocks that Matlab has optimized in terms of configuration but still ensure good signal processing function.

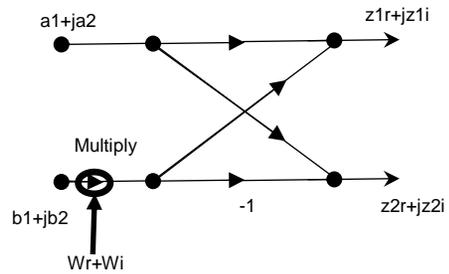


Figure 6. Butterfly Radix-2 (Functional diagram 2)

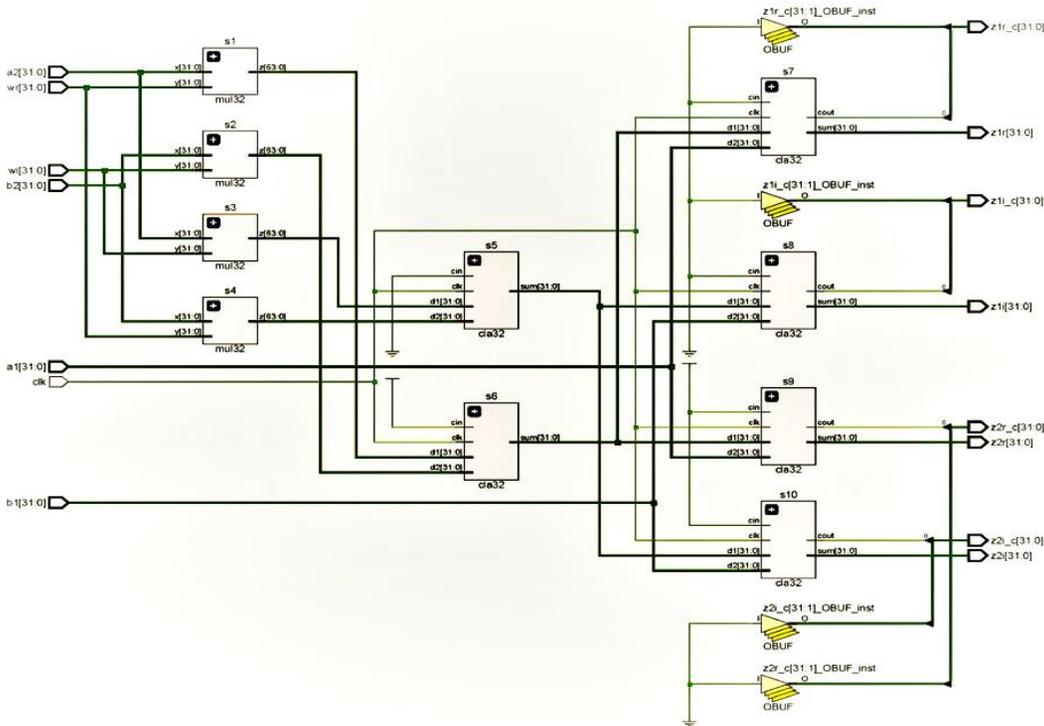


Figure 7. Butterfly Radix - 2 schematic using Vivado (schematic 2)

Name	Slice LUTs (17600)	Slice Registers (35200)
butterfly	5843	192
s5 (cla32_0)	635	32
s6 (cla32_1)	588	32
s7 (cla32_2)	70	32
s8 (cla32_3)	69	32
s9 (cla32_4)	34	32
s10 (cla32)	36	32

Figure 8. Resource utilization for figure 7

If we use Verilog programming to create the Butterfly block directly in Vivado, we have the schematic in Figure 7, using up to 10 blocks $s_1 \rightarrow s_{10}$, which are the Mul32 blocks (This is to multiply twiddle factor with the second number, that is also a complex number multiplication so it

needs 4 normal multiplications $s_1 \rightarrow s_4$) and are also 6 Cla32 blocks $s_5 \rightarrow s_{10}$ (This is to add/sub the product of multiplication to the first number). Each Cla32 block contains up to 8 Cla4 blocks, each containing up to 27 ports can be AND, OR, XOR. Therefore, the circuit created directly at Vivado will be more complicated in terms of the number of devices, compared with Sysgen. Moreover, if you look from Figure 5 and Figure 8, we see the number of Slice LUTs in schematic 1 is lower than that of schematic 2 compared schematic 1 is more reasonable because Slice LUTs (Look-Up Tables) are expensive and not

convenient to use as Slice Registers while the computational algorithms of the two schematics are completely the same.

5. CONCLUSION

Using the same Butterfly processing algorithm, the author uses two schematics: one from Sysgen blockset blocks and then transferred to Vivado and the other one implemented directly from Vivado. The conversion scheme using Blockset in Sysgen (schematic 1) is more reasonable than the direct implementation in Vivado due to the more optimised configuration and the use of Slice LUT less than the direct Vivado - using design scheme (schematic 2).

TÀI LIỆU THAM KHẢO

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Biography:



Tran Hoai Trung was born in 1976. He got Bachelor degree in University of Transport and Communications (UTC) in 1997 and hold the post of lecturer at the University. He then got a Master degree from Hanoi University of Science and Technology (HUST) in 2000. In the period 2003 to 2008, he had concentrated on researching in the field of Telecommunication engineering and got his PhD at University of Technology, Sydney (UTS) in Australia. He is currently lecturer at the UTC. His main research interests are digital signal processing (DSP), applied information theory, radio propagation, MIMO antenna techniques and advanced wireless transceiver design.



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