APPLICATIONS OF TCAD SIMULATION SOFTWARE TO THE STUDY OF FLOATING-GATE DEVICE

Dang Cong Thinh[1], *Mai Tri Hao*[1], *Hoang Trang*[1]

Abstract

The floating-gate device has become an established component of all electronic systems, especially Non-volatile memories in recent years. This paper produces a study for this device including the structure and operation (read, program/write and erase). A complete flow which uses ATHENA, ATLAS and DEVEDIT3D tools for 2D and 3D structure simulations including I-V characteristics, Channel Hot Electron Injection, and Fowler-Nordheim Tunnel simulations are performed in TCAD environment.

Index terms

Floating-gate device; Non-volatile memory; flash memory; Channel Hot Electron Injection; Fowler-Nordheim Tunnel; CMOS Process; TCAD.

1. Introduction

THE CMOS technology has been developed in the past several decades. Many novel circuit design techniques have been presented ranging from radio-frequency integrated circuits design [1]-[2] to millimetre-wave IC design [3], [4].

Over this period of time, there has also been a significant increase in the semiconductor memory market including volatile memories (SRAM or DRAM) and non-volatile memories (EPROM, EEPROM or Flash), and both of them are developing based on the complementary metal oxide semiconductor (CMOS) technology. Volatile memories lose data contents when power supply is turned off and non-volatile ones are capable of keeping data contents even without power supply. Thanks to this characteristic, the non-volatile memories offer the system many different opportunities and cover a wide range of applications such as cell phones, computers and communication [5]. Therefore, this kind of memory has been using commonly and it attracts great attention from many researchers. However, in order to study this kind of memory, we have to research the floating-gate device because it is the core of almost every modern non-volatile memories [6].

Many researches have been conducted to study the floating-gate device such as the 3D TCAD simulations of geometry effects on the floating-gate structure [7] which also

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demonstrate the floating-gate structure and parameter definitions in CMOS 180 nm technology or the simulations of threshold voltages of the floating-gate device between operations using TCAD tools [8]. However, all of these researches have not proposed a detailed flow to fabricate the floating-gate device. A detailed fabrication flow needs to be investigated firstly in simulation to save the time and the cost of fabrication.

In this paper, a detailed design flow to fabricate the floating-gate device is proposed to investigate the 2D and 3D structure and operation. The 2D structure allows the complete simulation of the operation of the floating-gate device, so it will be analyzed in detail while the 3D structure will be generally presented in this paper.

This paper includes 4 sections presented as follows: The structure of the floating-gate device is given in section 2. This section also presents the detailed operation of the floating-gate device including reading, programming, and erasing. Programming is performed by Channel Hot Electron current and erasing is performed by Fowler-Nordheim Tunnel current. Section 3 shows the detailed flow chart to fabricate a floating-gate device and the results of designing the 2D and 3D structures of the floating-gate device. The device operation simulation and analyzing simulation results at programming and erasing states are presented in section 4. The last section gives the conclusion.

2. Floating Gate Device

Floating-gate devices are at the core of almost every modern non-volatile memories [6]. Non-volatile memory describes a system where the contents of the memory are retained after the power is switched off. In silicon integrated circuit technology, non-volatile memories are realized through the use of an electrically isolated “floating gate”, which is electrically isolated from the gate and substrate by an insulator. A cross-section schematic shown in Figure *1* illustrates a floating-gate device [9]. The state of this device depends on the charge on a floating gate. These states are reading, programming (writing) and erasing. More importantly, the insulator around the floating gate must be thick enough to prevent the floating gate from discharging when the power is removed, and it also must be thin enough to allow the transfer of charge on and off the floating gate under appropriate bias configuration.

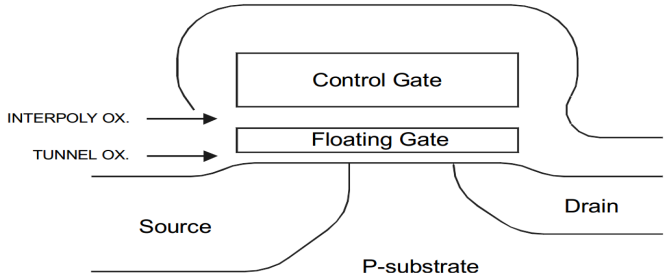
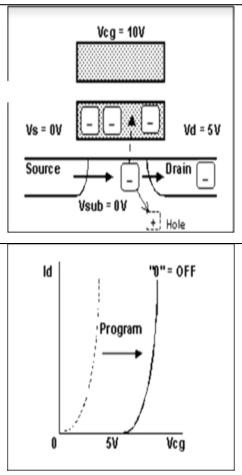
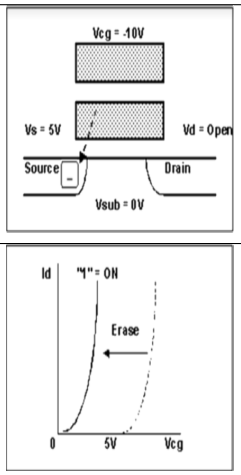
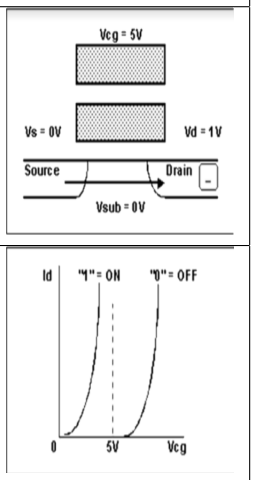


Fig. 1. *Cross section schematic of a floating-gate device*

Table 1. *Floating-gate device operations*

Program (Write) [Channel Hot Electron Injection]	Erase [Fowler Nordheim Tunnel]	Read
		

The operations of the floating-gate device are presented in the following table [10].

Programming refers to putting charge on the floating gate, erasing refers to removing the charge from the gate, and reading involves sensing the electrical signal of the cell to determine if the device is programmed or erased.

2.1. Read Operation

The read operation is performed by applying a gate voltage that is between the values of the erased and programmed threshold voltages and sensing the current flow through the device [6].

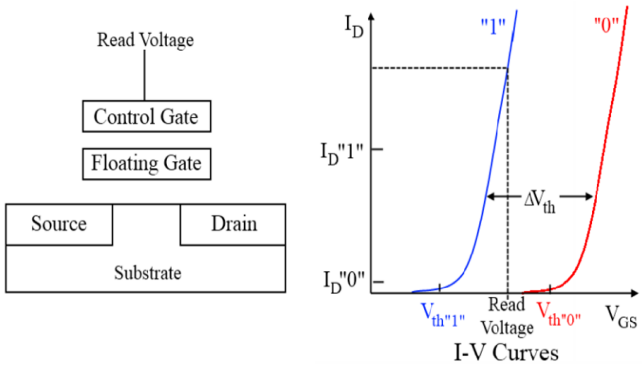


Fig. 2. *Floating-gate reading operation*

In Figure 2, V_{th}"1" is the threshold voltage of the floating-gate device at the erasing state and V_{th}"0" is the threshold voltage of the floating-gate at the programming state. The threshold voltage shift ΔV_{th} is determined according to the formula below:

$$\Delta V_{th} = \frac{-(Q_{th}"0" - Q_{th}"1")}{C_{pp}} \tag{1}$$

where $Q_{th}"0"$ is the charge on the floating gate when the floating-gate device at programming state, $Q_{th}"1"$ is the charge on the floating gate when the floating-gate device at erasing state, C_{pp} is the capacitance between the control gate and floating gate.

2.2. Program Operation

The program operation is performed when electrons move from the substrate to the floating gate. These electrons are called Channel Hot Electrons. The Channel Hot Electron current includes the CHE and the CHISEL currents.

Qualitatively, to contribute to CHE and CHISEL currents, such electrons must gain from the lateral field sufficient kinetic energy to be able to overcome the Si/SiO_2 barrier, and their momentum has to be directed toward the gate for the hot electrons to be collected at the gate [6]. The program operation is illustrated in Figure *3*.

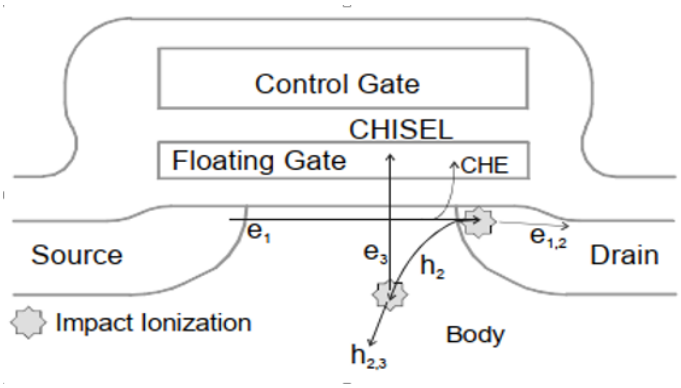


Fig. 3. Floating-gate programming operation

2.3. Erase Operation

The erase operation is performed when electrons move from the floating gate cross the tunnel oxide to the substrate under the appropriate bias configuration. The electron current is called Fowler-Nordheim Tunnel current [6]. The figure bellow demonstrates the configuration for erase operation.

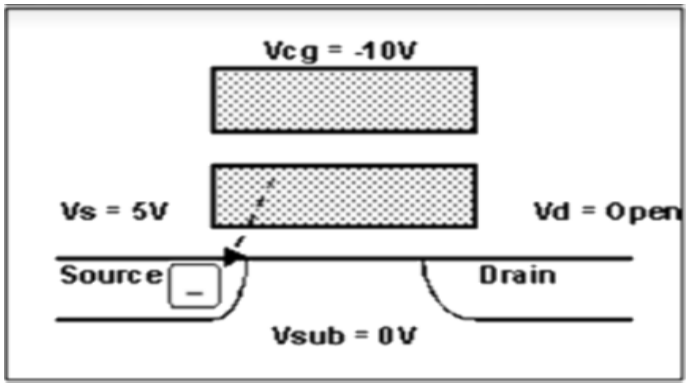


Fig. 4. Floating-gate erasing operation

3. Floating Gate Fabrication Steps

The detailed process flow to fabricate a floating-gate device with P-type substrate for 180nm CMOS process is presented in Figure *5*.

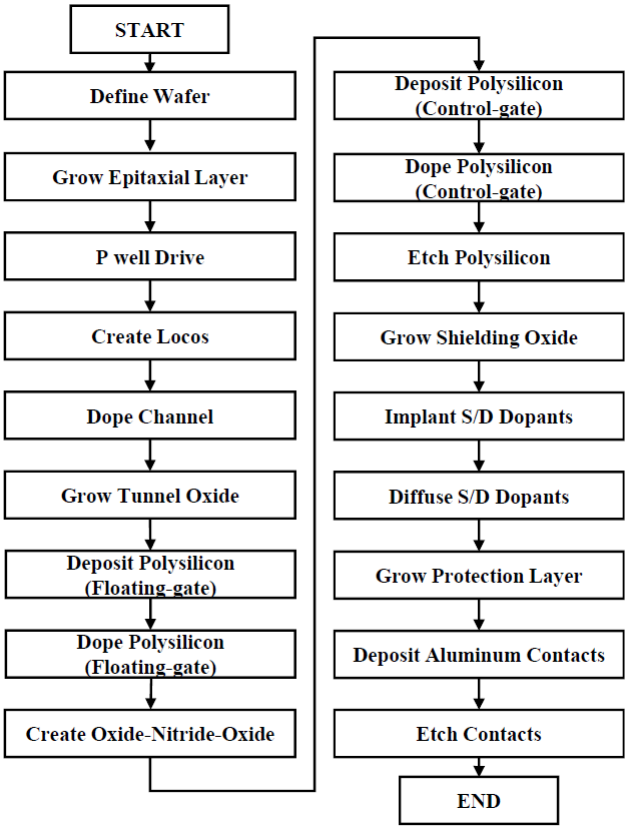


Fig. 5. Floating-gate device design flow chart

This flow proposes using an addition Epitaxial grow layer which was not used in

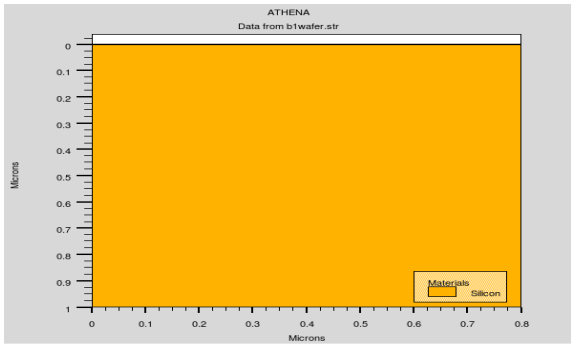
traditional CMOS processes. The growth of an epitaxial layer over the P-type substrate offers some advantages including improving the performance of this device as well as floating-gate integrated circuits, minimizing latch-up effects that a CMOS circuit may undergo when powered up, and helping control the doping concentration of this device accurately [11].

The main difference in terms of structure between the floating-gate device and CMOS device is that the floating-gate device has an additional floating gate which is created by two steps: Deposit Polysilicon (Floating gate), Dope Polysilicon (Floating gate) in the flow.

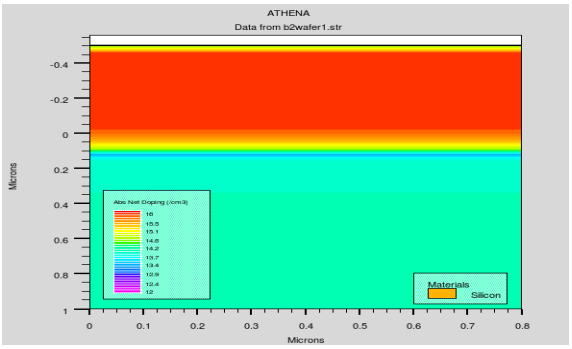
These figures below illustrate the main process simulations using TCAD based on the design flow chart presented above (Figure *6*a-*6*h).

ATHENA is used to generate a mesh to simulate 2D CMOS process including the structure, doping profile, and contact area. ATHENA provides general capabilities for numerical, physically-based, 2D simulation of a semiconductor process. It can perform structure initialization and manipulation, basic deposition, etch facilities, and user-defined model for implantation and diffusion [12].

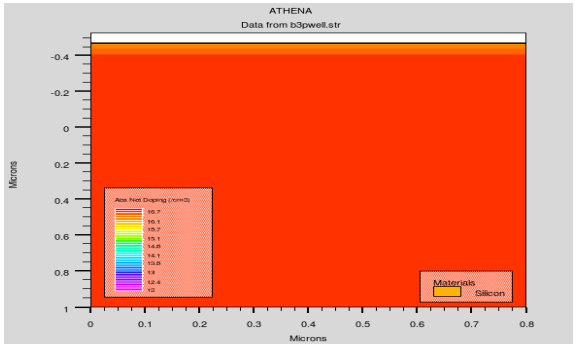
The fabrication process starts from creating P-substrate (initial surface thickness = $1\mu m$) with Boron at a concentration of 1.0e14 cm^{-3} (Figure *6*a). Next, a mesh is defined, and the density of the mesh is a trade-off between accuracy and simulation time. After the mesh and wafer definition, a $0.45\mu m$ thick Epitaxy layer with Arsenic at a concentration of 1.0e16 cm^{-3} is grown on the top to make device surface thickness increase to $1.45\mu m$ (Figure *6*b). Then, a P well is implanted using Boron with a dose of 8e12 cm^{-3}. After that, the P well is also diffused with Nitro gas at 1200^{o}C for about 310 minutes (Figure *6*c). Next, Locos and tunnel oxide layer are created (Figure *6*d). Creating Locos is an important step in the fabrication of semiconductor devices for the purpose of isolating the operation of two devices on the same wafer, and Oxide is usually used for this isolation. The doping channel is created using Boron at 100KeV and a concentration of 2.5e12 cm^{-3} (Figure *6*e). Figure *6*f shows the device structure after Polysilicon (Floating gate) is deposited and doped. Figure *6*g shows the device structure after Polysilicon (Control gate) is deposited and doped. The Floating gate, Control gate, Tunnel Oxide layer and Oxide-Nitride-Oxide layer which is between Floating gate and Control gate are etched. An oxide layer with a thickness of $0.1\mu m$ is deposited and etched on the top to protect the device by the next steps. The next step is to create Source and Drain gates with Arsenic at 50 KeV and a concentration of 7e12 cm^{-3} (Figure *6*h). After growing the protection layer, the final step is to deposit and etch Aluminum contacts for Source and Drain gates. The complete 2D floating-gate device is presented in Figure *7*.



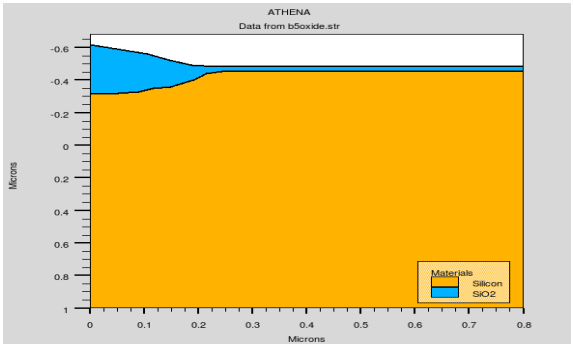
(a) Definition wafer



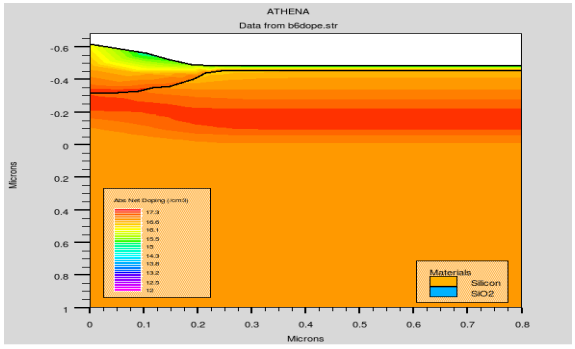
(b) Grow Epitaxial layer



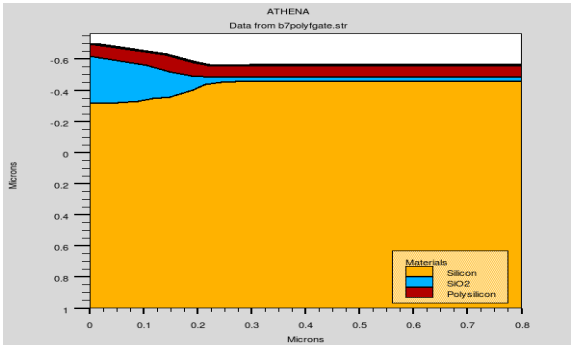
(c) P well drive



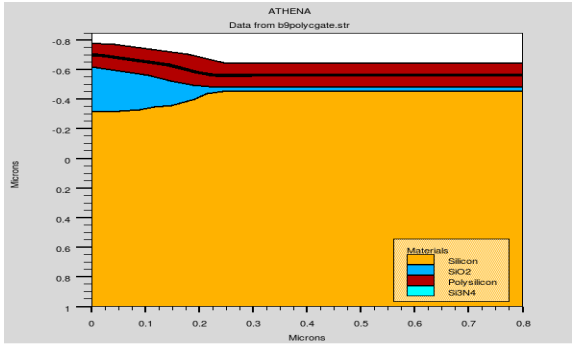
(d) After creating Locos and grow Gate oxide



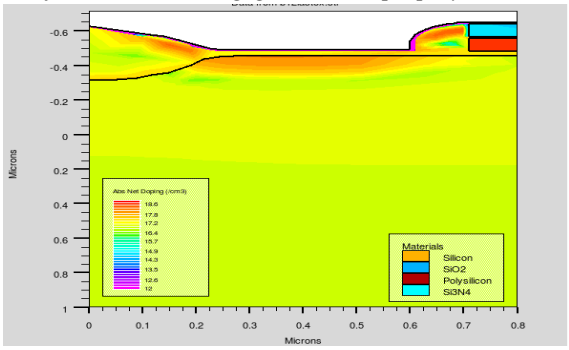
(e) Dope channel



(f) Create Floating gate and dope polysilicon



(g) Create Control gate and dope polysilicon



(h) After implant and diffuse S/D dopants

Fig. 6. The main process simulations with TCAD including in a) Definition wafer b) Grow Epitaxial layer c) P well drive d) After creating Locos and grow Gate oxide e) Dope channel f) Create Floating gate and dope polysilicon g) Create Control gate and dope polysilicon h) After implant and diffuse S/D dopants

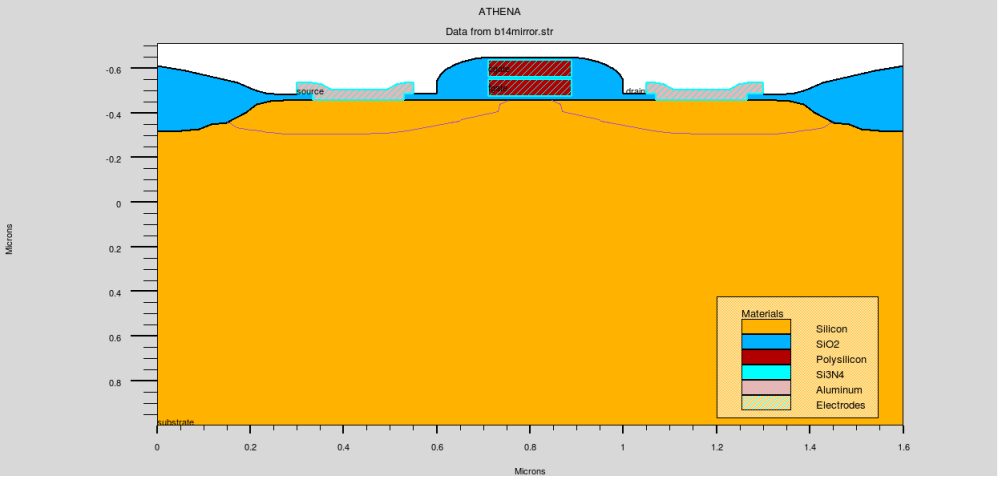


Fig. 7. The 2D structure of the floating-gate device

The 3D structure of the floating-gate device is created from the 2D structure and the value of width by using DEVEDIT3D tool. The 3D structure of the floating-gate device is shown in Figure *8*.

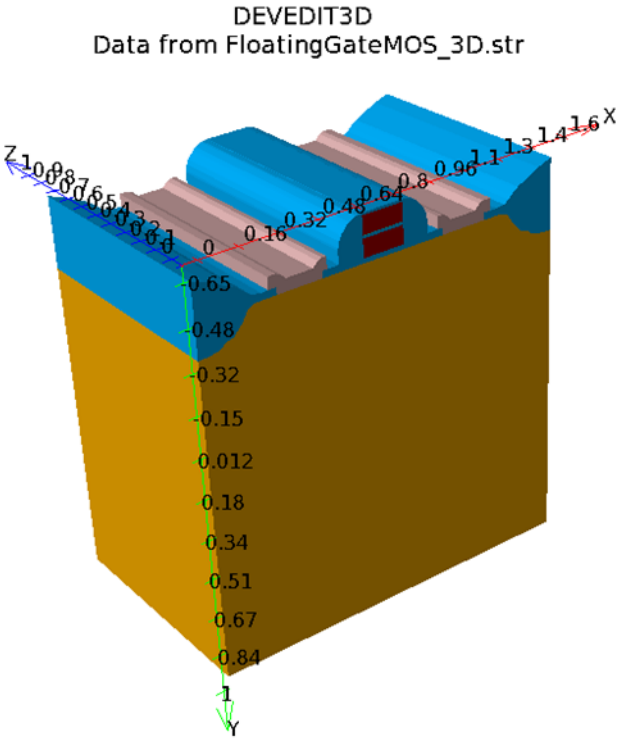


Fig. 8. The 2D structure of the floating-gate device

4. Simulation Results

ATLAS is a physically-based two and three-dimensional device simulator that predicts the electrical behavior of semiconductor devices at specified bias conditions. The physical structure created using ATHENA tool is used as the input for ATLAS tool. The combination of ATHENA and ATLAS makes it possible to simulate and extract the device characteristics [12]. These figures below show the characteristics of the floating-gate device at the programming state and the erasing state.

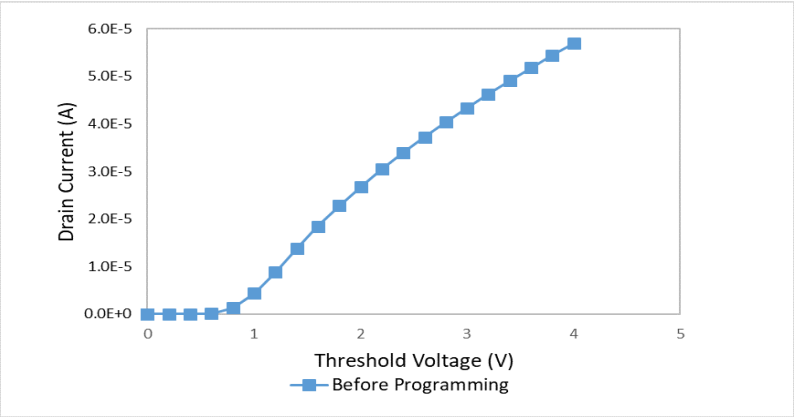


Fig. 9. Threshold voltage before programming

Initially, no charge is stored on the floating-gate (Q = 0) and before programming, the threshold voltage of the floating-gate device is 0.6V (Figure *9*).

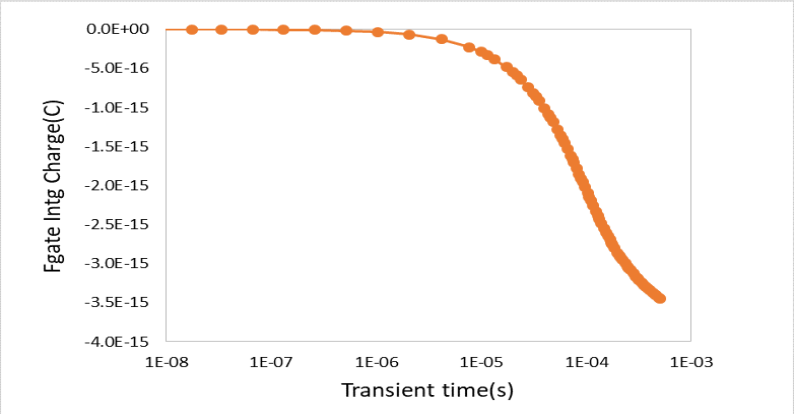


Fig. 10. Floating gate charge in programming

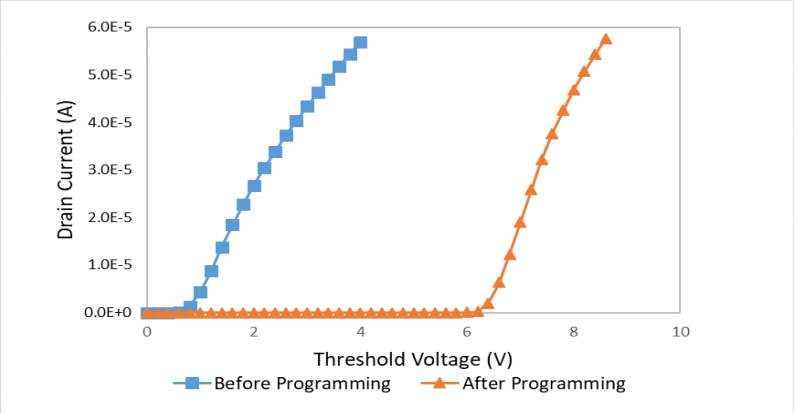


Fig. 11. *Threshold voltage after programming*

The transient simulation for the charge on the floating gate is shown in Figure *10*. In order to perform the simulation, the voltage of the Control gate is 12V, the Drain gate is 5.85V, and the Source gate is 0V.

The amount of negative charge on the floating gate increases from 0 (C) to -3.5e-15 (C) as the electron moves from the substrate to the floating gate. The electron flow consists of two currents CHE and CHISEL shown in Section 2. At the same time, after programming, the threshold voltage of the floating-gate device increases from 0.6V to approximately 6V (Figure *10-11*).

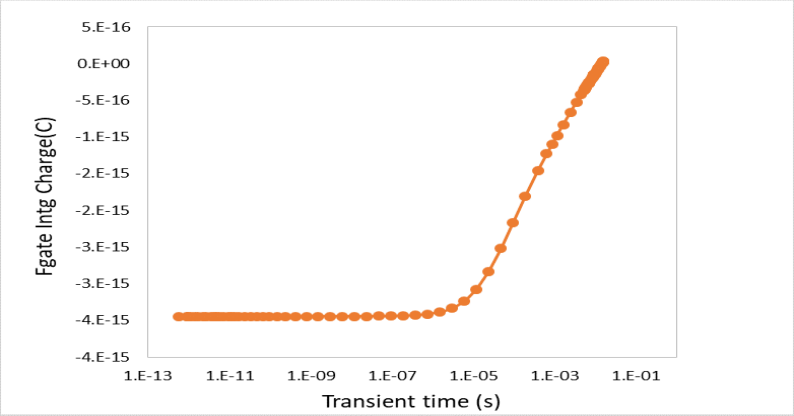


Fig. 12. *Floating gate charge in erasing*

To perform the transient simulation for the charge on the floating gate during the erasing state, the voltage of the Control gate is -15V, the Drain gate is 0V, and the Source gate is 15V.

After erasing, electrons on the floating gate move from the floating gate to the substrate, causing the amount of charge in the floating gate to change from -3.5e-15 (C) to 0 (C). Fowler-Nordheim is the flow of electrons moving from the floating gate

to the substrate and presented in Section 2.

5. Conclusion

In this paper, a detailed design flow chart is suggested to fabricate the floating-gate device in TCAD environment. This paper is successful in studying the structure and operation of the floating-gate device. All of the process steps including ATHENA, ATLAS, and DEVEDIT3D commands are performed to simulate the 2D and 3D structure and the device characteristics. The results of the transient programming and erasing simulations worked as expected.

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ỨNG DỤNG CỦA PHẦN MỀM MÔ PHỎNG TCAD TRONG NGHIÊN CỨU LINH KIỆN CỰC CỔNG NỔI

Tóm tắt

Trong những năm gần đây, linh kiện cực cổng nổi đã trở thành một thành phần thiết lập trong hầu hết tất cả các hệ thống điện tử, đặc biệt trong các bộ nhớ Non-volatile. Bài báo này đưa ra một nghiên cứu về cấu trúc và hoạt động (đọc, lập trình/ghi và xóa) của linh kiện cực cổng nổi. Một quy trình chế tạo cấu trúc 2D và 3D hoàn chỉnh cho linh kiện cực cổng nổi sử dụng công cụ ATHENA, ATLAS và DEVEDIT3D được đề xuất trong bài báo này. Các mô phỏng bao gồm đặc tính I-V, Channel Hot Electron Injection, và Fowler-Nordheim Tunnel được thực hiện trong môi trường TCAD.